OCEAN TOMO

全球专利在线竞价交易市场

LOT #167

Semiconductor Manufacturing Test

OCEAN TOMO

BID-ASK™ MARKET

IP Intro.

Patented Technology Introduction

for System IC Semiconductor Manufacturing Test Time and Cost Reduction

Ver.03

10/03/2022

iNNOTiO Inc.

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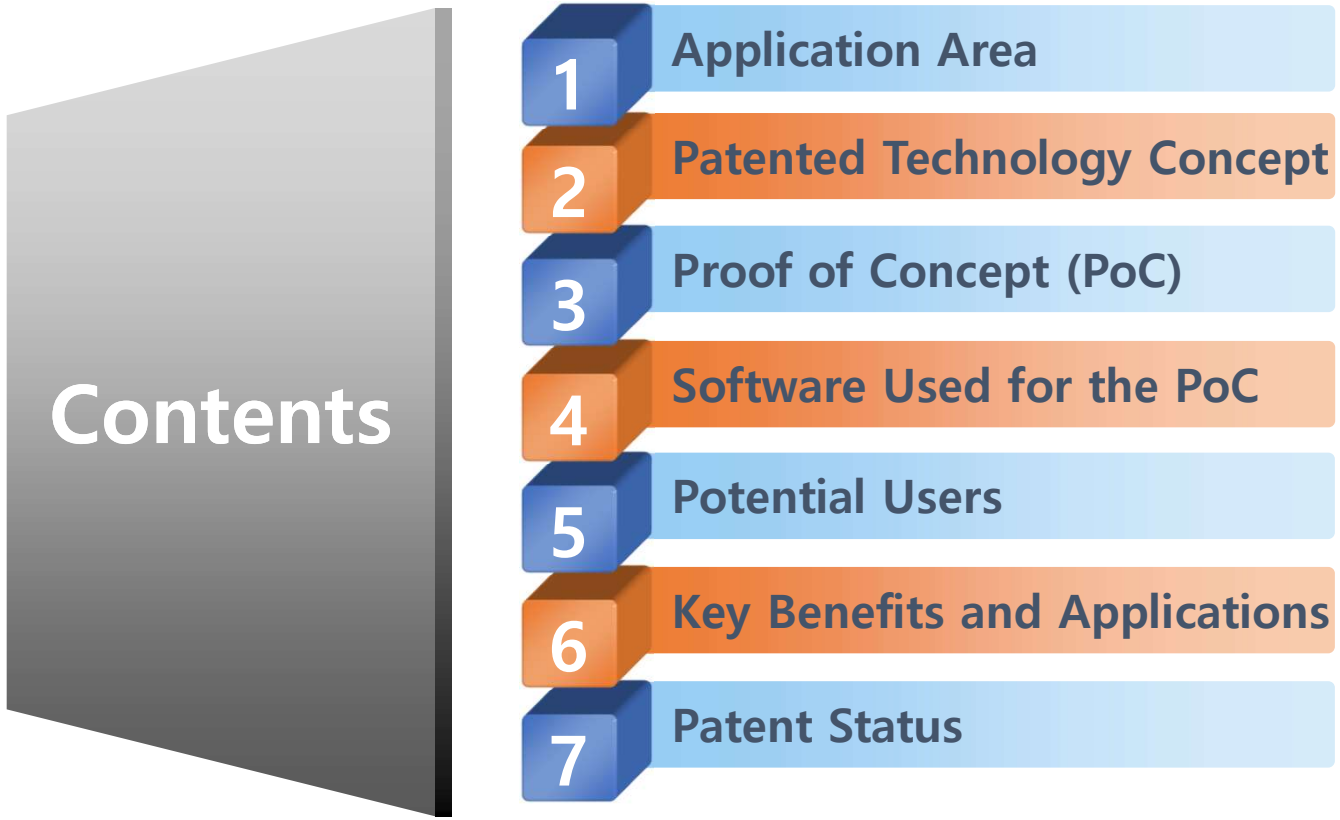


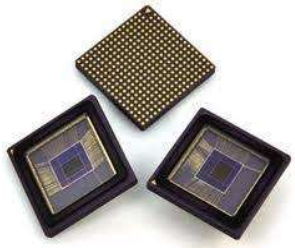
1. Application Area (1)

The main application area of our patented technology is system IC manufacturing test time and cost reduction.

System IC Manufacturing Test

■ Manufacturing Test :
Classification of good and defective device

wafers



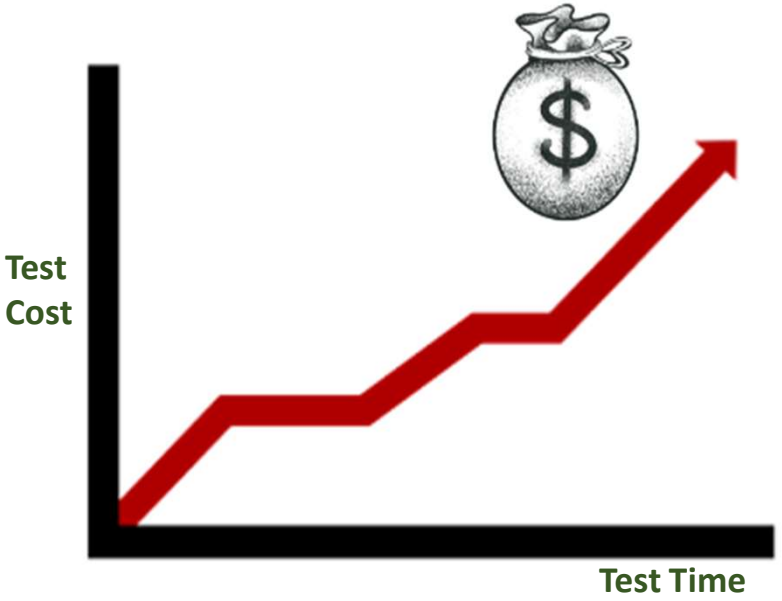
Packaged Chips

- wafer test
- package test
- system level test
- burn-in test
- temp. test (hot/room/cold)

Test Time and Cost

▶ Increase in Manufacturing Cost

▶ Increase in Time-to-Market



1. Application Area (2)

The patented technology's primary purpose is scan test time reduction.

- Scan test time accounts for about 20~50% of system IC test time, and the proportion is increasing as complexity increases, like AI chips.

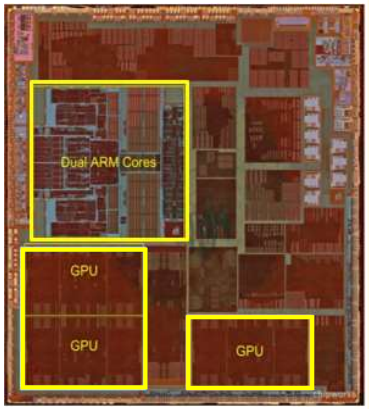
Scan Test

The scan test detects faults in digital circuits.

Automatic Test Equipment (ATE)

① Input of scan test data

② Output of scan test result data



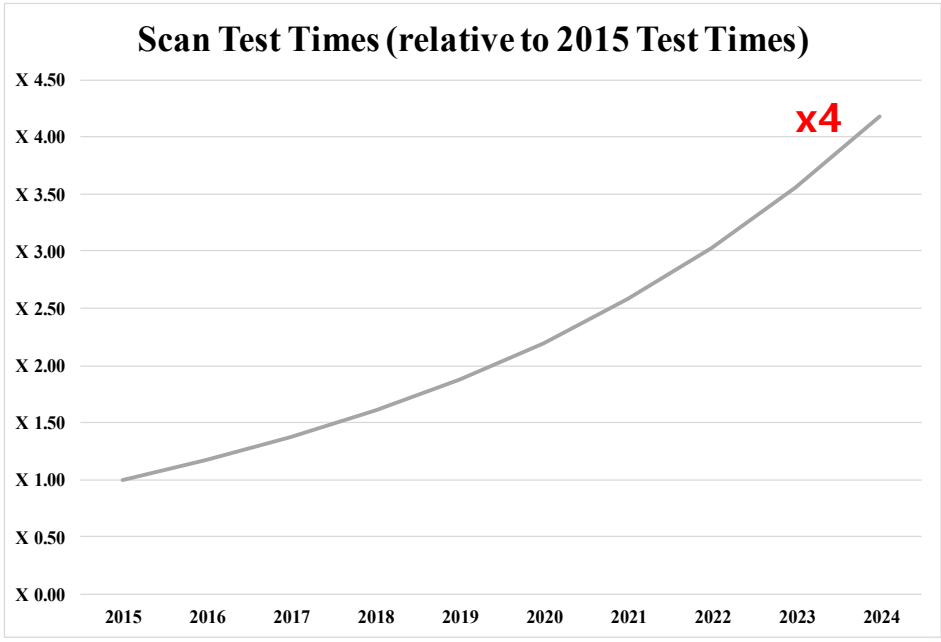
System IC

③ Pass/Fail decision after comparing expected result data and test result data

Scan Test Time Trend

SoC

As digital circuits become more complex and denser, the scan test time is increasing.

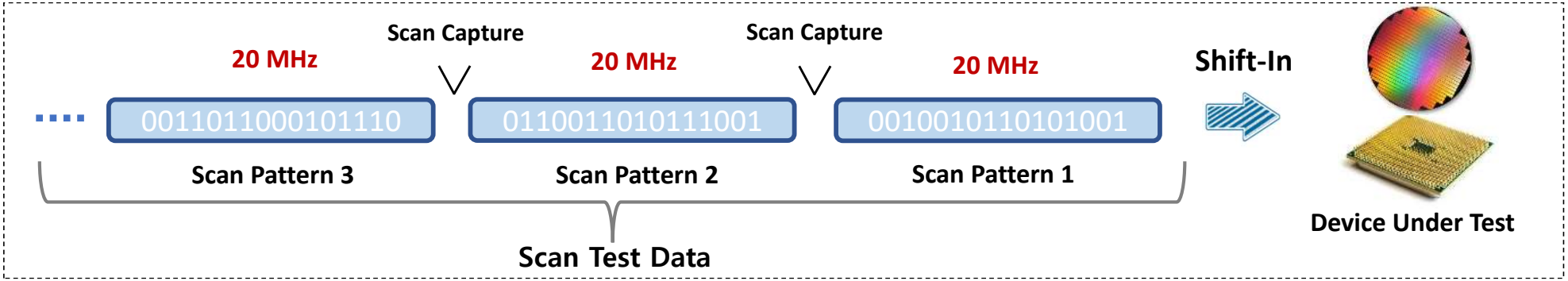


ITRS(International Technology Roadmap for Semiconductors), 2015

- The industry standard test method, scan test, is used to test whether a digital circuit is faulty.
- Various defects such as stuck-at-0, stuck-at-1, signal path delay, and signal transition delay can be detected by the scan test.

Traditional Scan Test

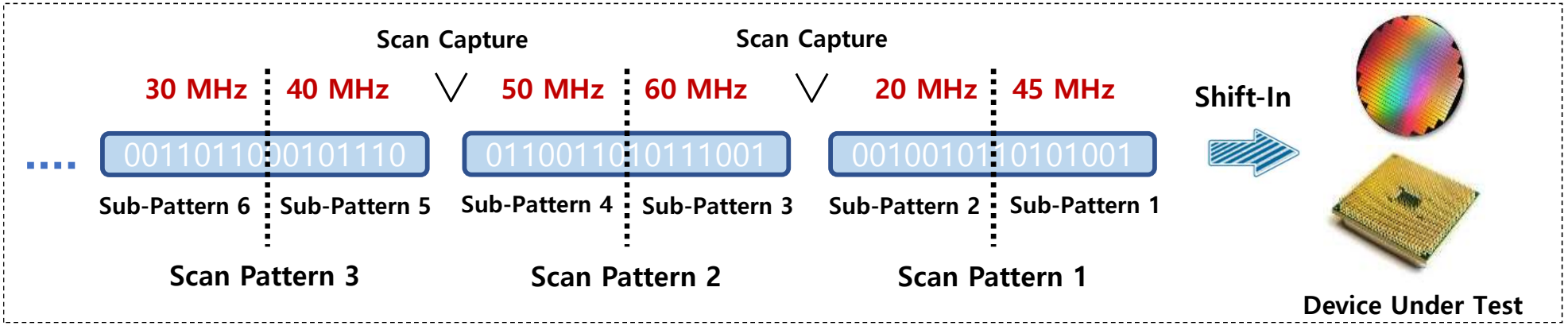
"Single low shift frequency is used for all scan patterns."



Scan Test by the Patented Technology

"Scan patterns are divided into scan sections, and optimal shift frequencies of the scan sections can be determined to reduce test time."

- Scan section : a scan pattern set or a scan sub-pattern



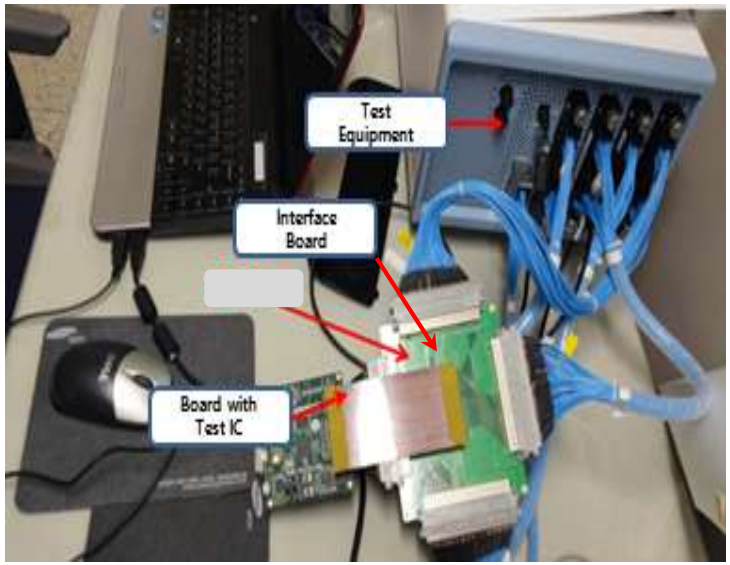
3. Proof of Concept (PoC)

PoCs of the patented technology were performed by using our Veloscan® software.

ADVANTEST®

The PoC of the patented technology was performed using CX1000D test equipment, a voice processor chip (target device), and our Veloscan S/W.

⇒ About 28~35% reduction in scan test time



TERADYNE

We performed a PoC of the patented technology with Teradyne Korea using UltraFlex Plus test equipment, an application processor chip (target device), and Veloscan S/W.

⇒ About 30% reduction in scan test time

Foundry

The PoC of the patented technology was successfully performed with a foundry company.

4. Veloscan Software Used for the PoC

Existing Automatic Test Pattern Generation (ATPG) Tool's Limit

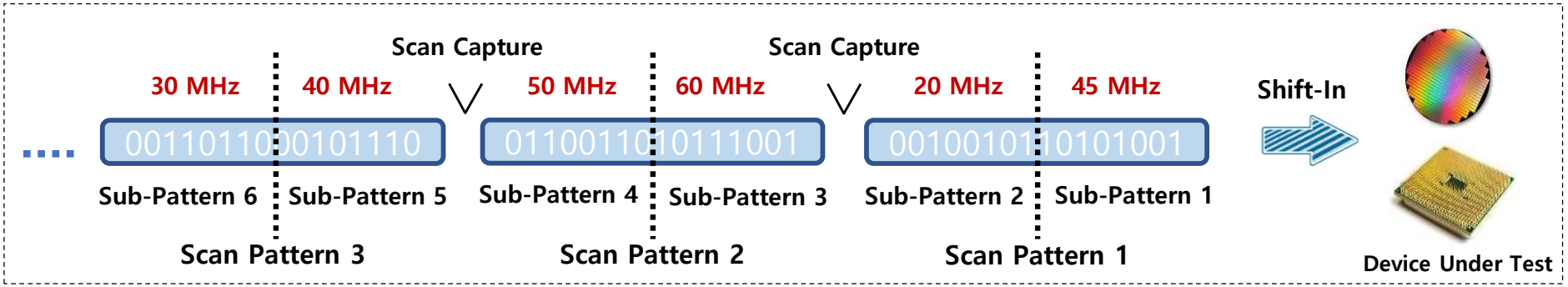
ATPG S/W generates a scan pattern data file by analyzing an IC design.

1. There is **no ATPG S/W optimizing the shift frequency of scan patterns** by dividing scan patterns into scan sections and supporting various scan shift frequencies.
2. There are **a lot of factors to determine the optimal maximum shift frequency** for each divided scan pattern.
   - Example of the factors: power, design issue, process variation, test environments, and so on.

Solved by Veloscan®

We have validated the patented technology using our software Veloscan®.

- **The software optimizes the original scan test data file so that the scan pattern data can be input to the device under test at the optimal frequency.**
- **Expected reduction ratio of scan test time : 10 ~ 30%**

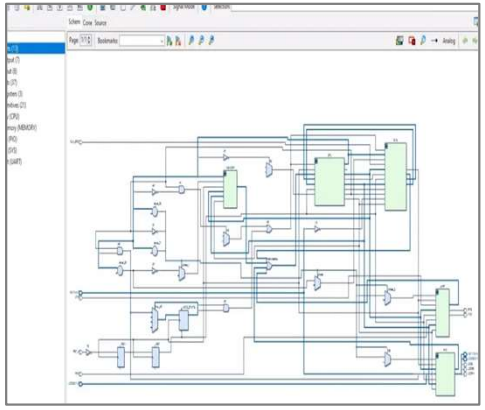


4. Veloscan Software Used for the PoC

Veloscan s/w can be used at a post-silicon stage.

Existing Software for Optimizing Scan Test

Pre-Silicon (Design Level) Tool



Scan design implementation and scan pattern file generation s/w tools

Pre-silicon Tools for Scan Test Optimization

- Design-for-Testability (DFT) Software
- Automatic Test Pattern Generation (ATPG) Software

Veloscan's Position

Post-Silicon Tool

Scan pattern shift frequency optimization s/w
(Scan pattern file optimization)

Post-silicon Tool for Scan Test Optimization

- Veloscan
  Scan Shift Frequency Optimization Software

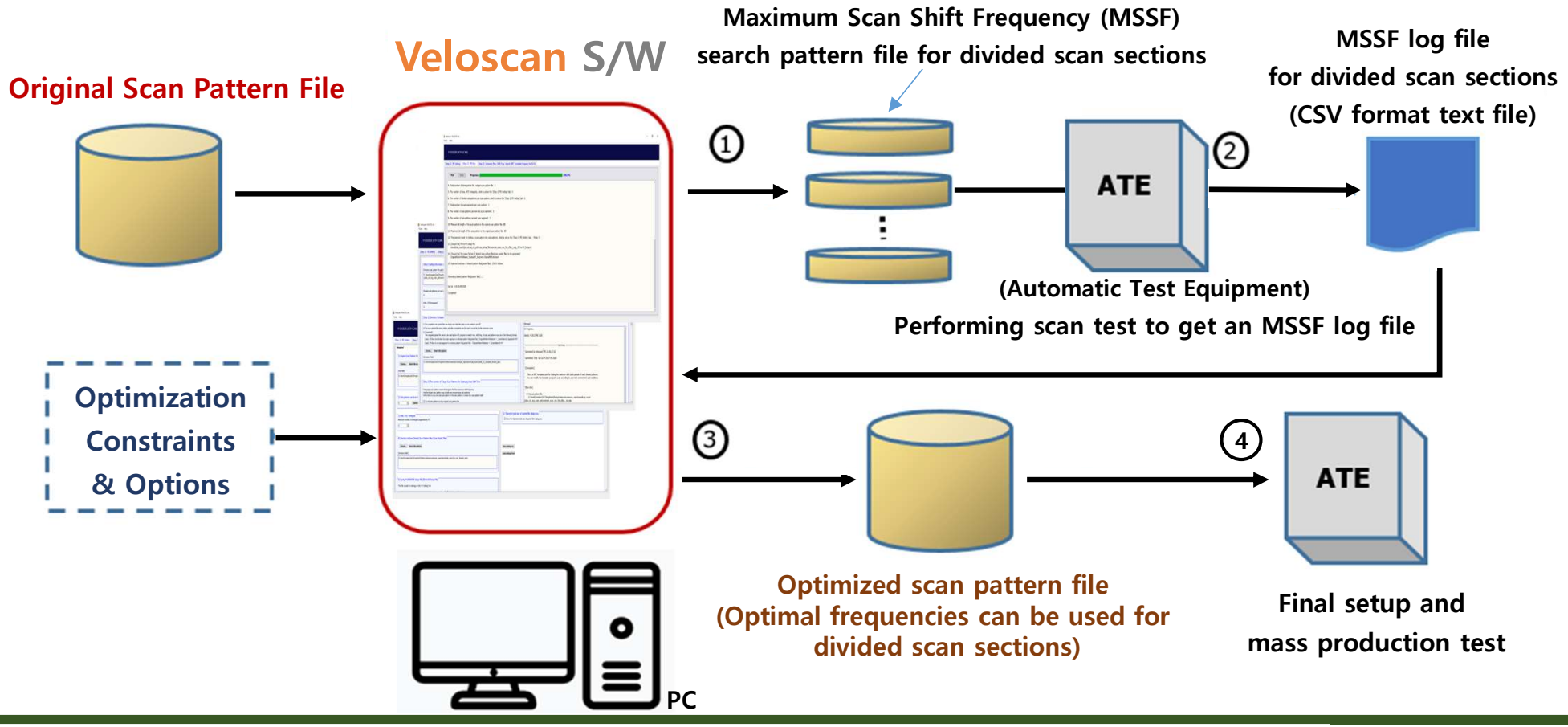
4. Veloscan Software Used for the PoC

Optimization Method Overview by Veloscan®

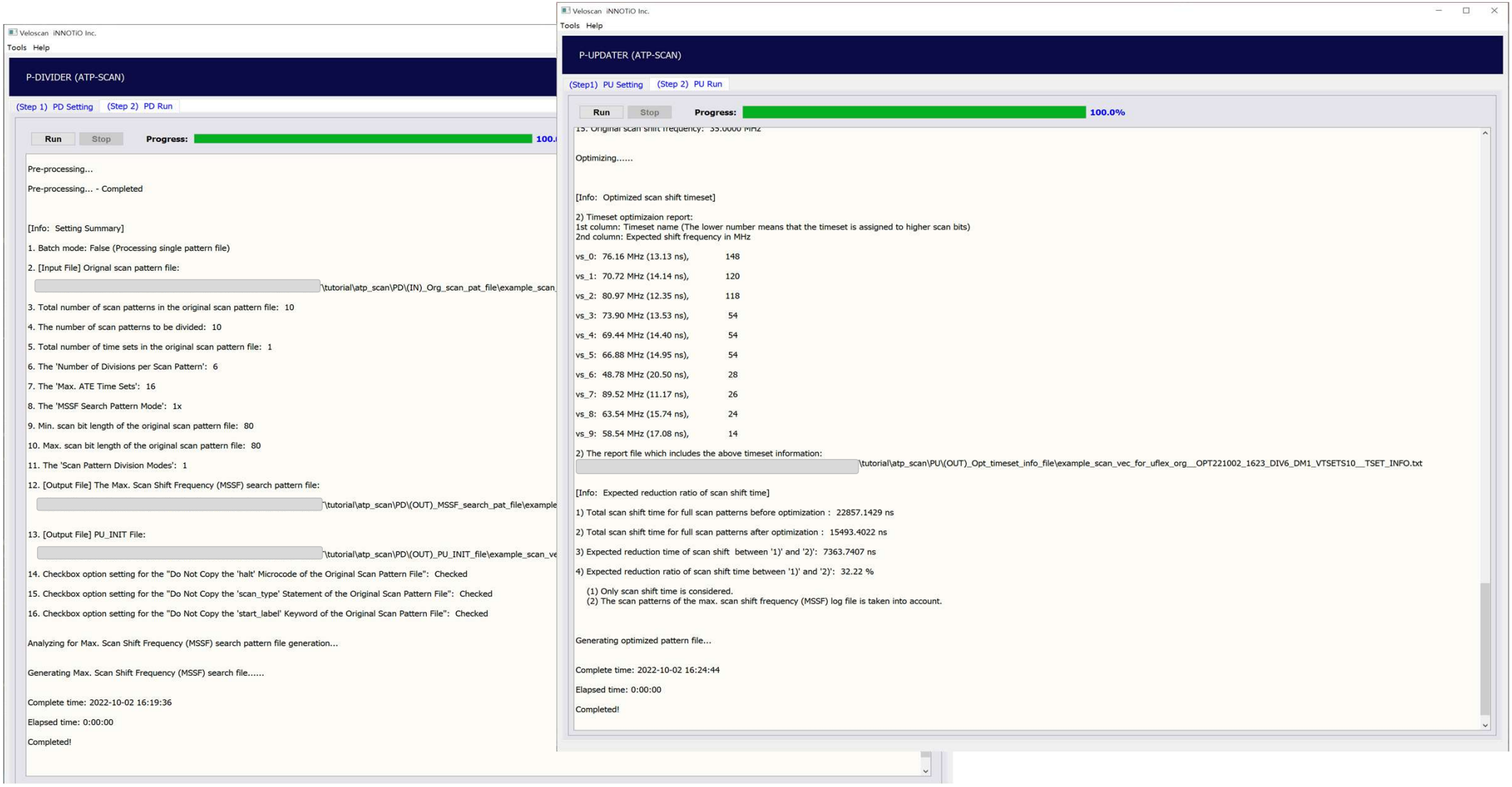
1. The Veloscan tool analyzes scan test pattern data and divides it into scan sections.
2. And the tool optimizes the assignment of timesets to the divided scan sections so that optimal frequencies can be used for the scan sections.

- The timeset defined in a test data file is an identifier used to control the frequency of a specific bit pattern section by an ATE. So, scan sections with the same timeset are controlled with the same frequency.

Optimization Flow by Veloscan®



Veloscan S/W screenshot



- **Supported ATE : Teradyne's UltraFLEX and UltraFLEX Plus (pattern file format: atp)**
- **Tested OS : Windows 7 (64 bits), Windows 10 (64 bits)**
- **Proven state : Silicon-level proven**

5. Potential Users

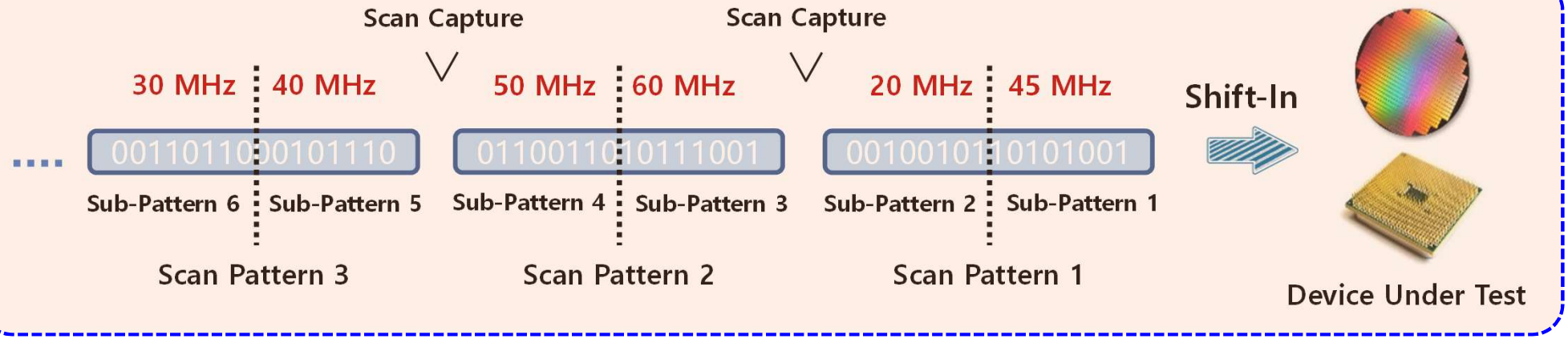
We believe that the patented technology would be helpful for effectively reducing system IC manufacturing test time, cost, and time-to-market.

Reducing Test Time and Cost

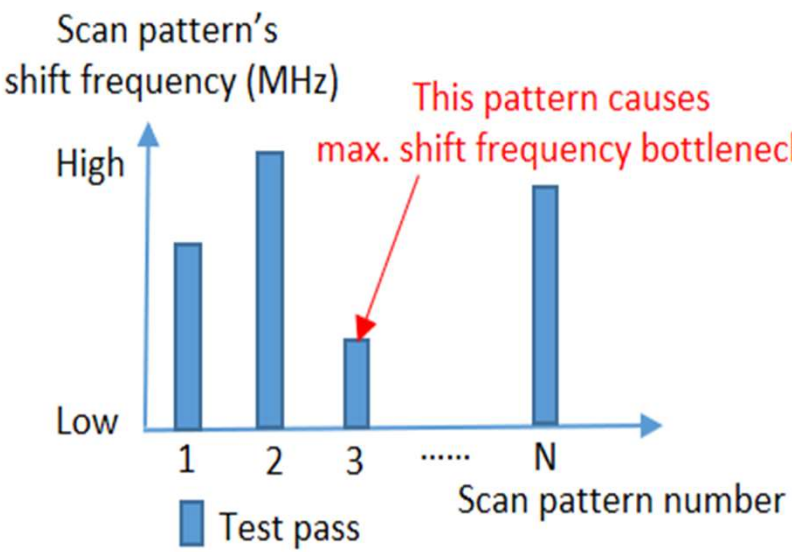
The patented technology can enable the reduction of scan test cost and time-to-market of system ICs by optimizing scan shift frequency at a post-silicon stage.

Scan patterns shift time that generally takes more than 90% of total scan test time can be significantly reduced (Refer to the PoC cases on page 5).

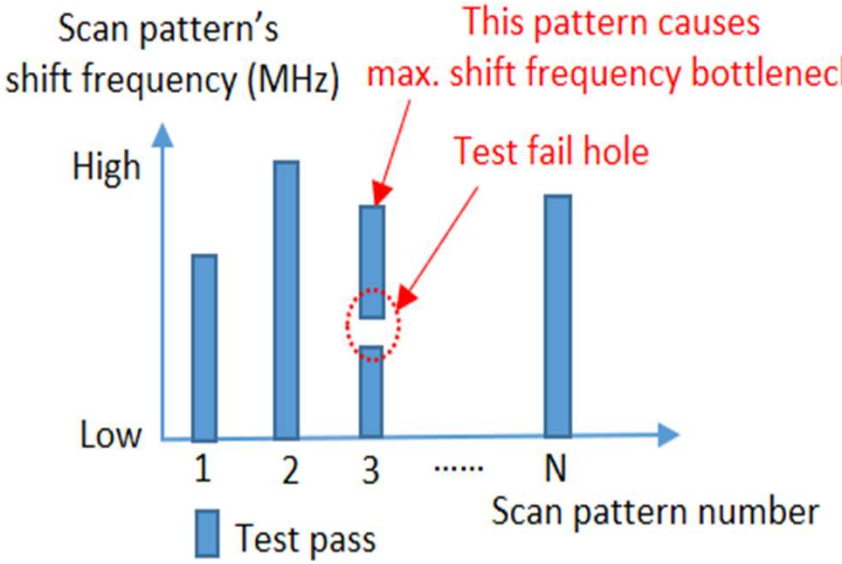
"Scan patterns are divided into scan sections, and optimal shift frequencies of the scan sections can be determined to reduce test time."



Efficiently Addressing the Scan Patterns Causing Test Setup Problems - (1)



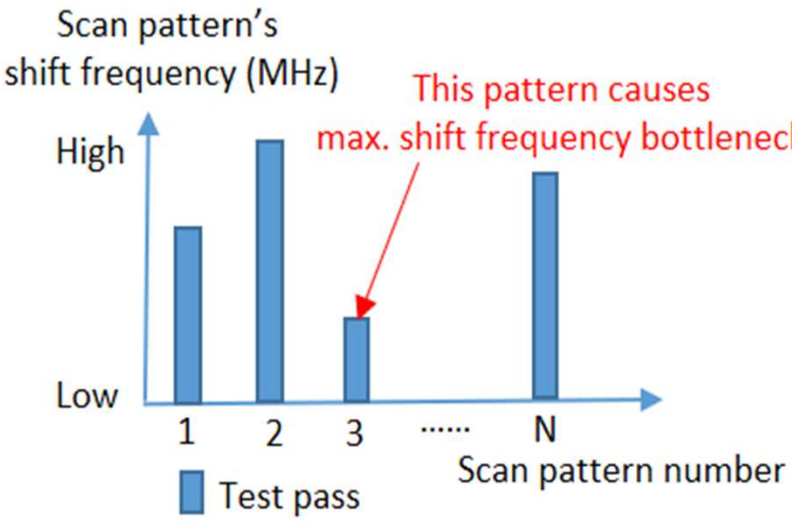
(a) Problem case 1



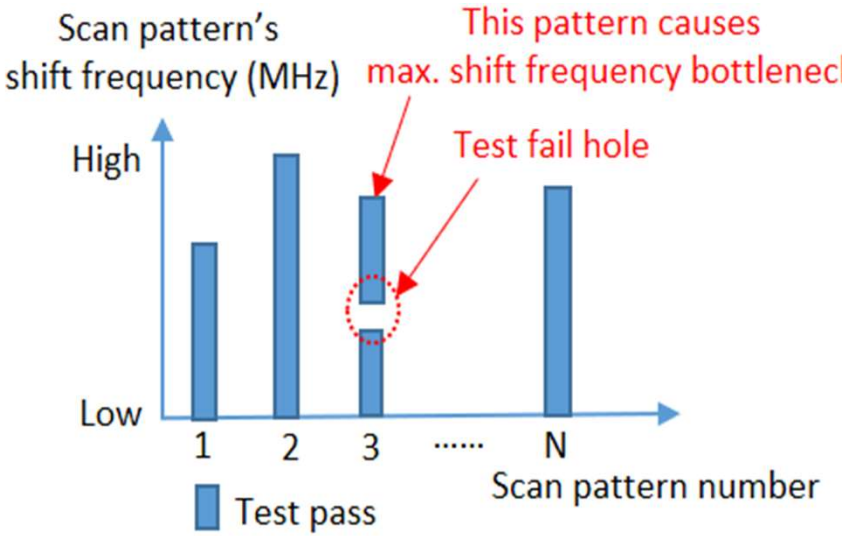
(b) Problem case 2

During scan test setup using ATE and device under test (DUT), the scan pattern problems can occur, such as causing a scan test to fail over a wide range of shift frequencies (figure (a)) or a scan test to fail between two scan test pass frequencies (figure (b)).

Efficiently Addressing the Scan Patterns Causing Test Setup Problems - (2)



(a) Problem case 1



(b) Problem case 2

To address the above problem cases (figure (a) and (b)), instead of taking much time and effort such as diagnosing, debugging, pattern masking, and lowering the shift frequency of whole scan patterns, the patented technology, and Veloscan can efficiently address the problems by using optimal scan shift frequency for each divided scan section (a scan pattern set or a scan sub-pattern) and provide the following benefits.

① **Fault coverage can be kept high by minimizing pattern-masking usage that excludes certain scan patterns from testing. And also, field escapes of defective devices can be reduced.**

② **Test time increment can be minimized by not lowering the shift frequency of whole scan patterns.**

6. Key Benefits and Applications (4/4)

Considering All Factors Affecting Scan Test

As a post-silicon solution, all real-world factors affecting a scan test are considered together for optimizing the shift frequency of divided scan sections (scan patterns or scan sub-patters) to reduce total scan test time.

No Change of IC Design

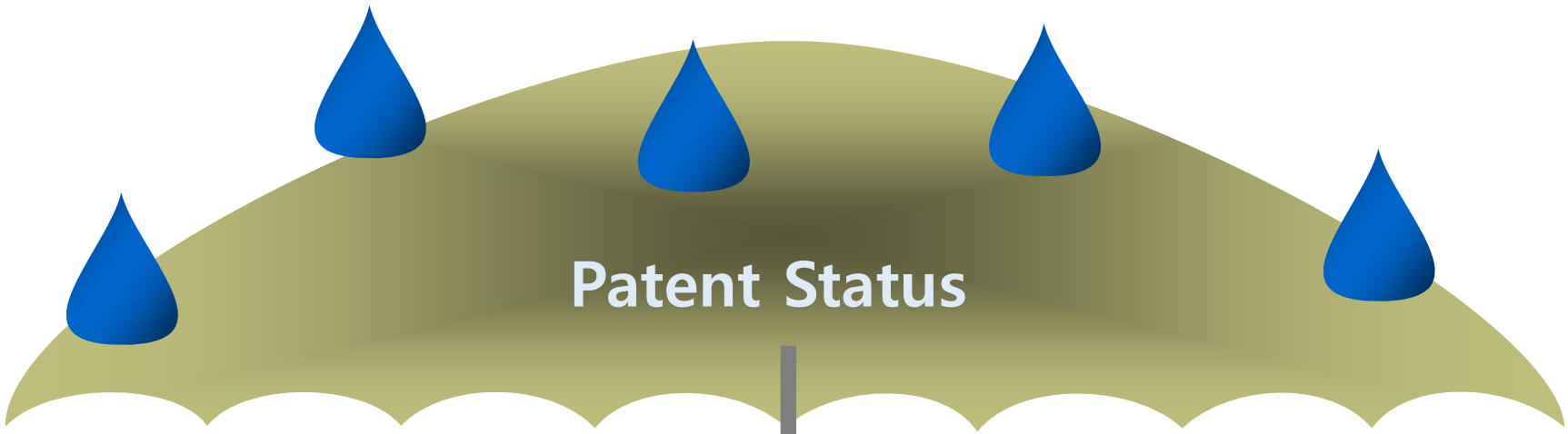
There is no impact on IC design.

No Change of Original Scan Test Data

The test data of an original scan pattern file is not changed.

Scan-Shift-Frequency-based Characterization

The Max. Scan Shift Frequency (MSSF) log for divided scan patterns can be used as a scan-shift-frequency-based characterization data. And the MSSF log file may be used in conjunction with other EDA tools for design, process, and yield improvements.



Country/PCT	Total	Registered	Filed
Korea	8	6	2
USA	3	3	-
Japan	1	1	-
Taiwan	1	1	-
Singapore	1	1	-
China	1	1	-
PCT	1	-	1
Total	16	13	3

Thank you!

Contact

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